



atomera

Investor Presentation

May 2021

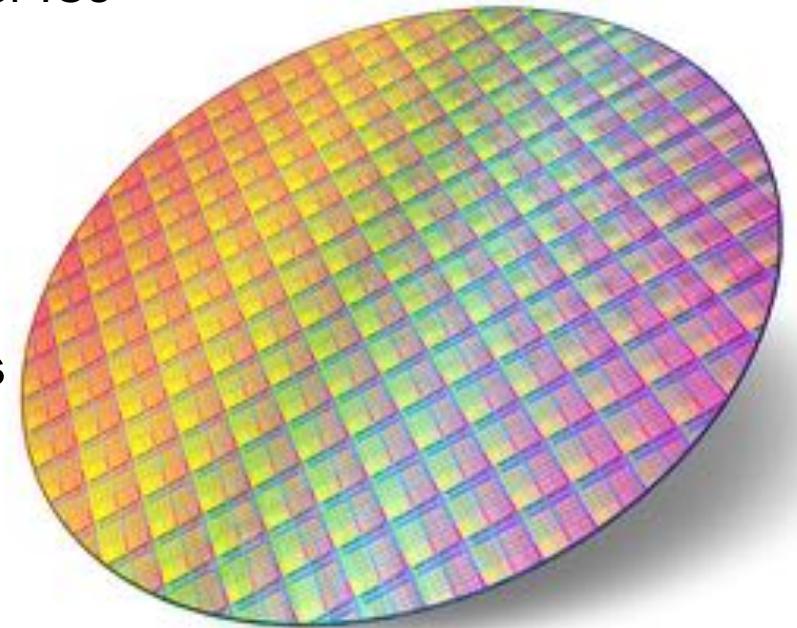
This presentation contains forward-looking statements concerning Atomera Incorporated (“Atomera,” the “Company,” “we,” “us,” and “our”). The words “believe,” “may,” “will,” “potentially,” “estimate,” “continue,” “anticipate,” “intend,” “could,” “would,” “project,” “plan,” “expect” and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those disclosed in the section “Risk Factors” included in our Annual Report on Form 10-K filed with the SEC on February 19, 2021. In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements as predictions of future events. Although we believe that the expectations reflected in our forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

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Investment Overview



- ▶ **Mears Silicon Technology (MST®) is a thin film used to enhance semiconductors**
 - Results in higher performance, lower power, and lower costs for ICs
- ▶ **Capital-light IP and technology licensing business**
 - Robust and growing patent portfolio
- ▶ **Engaged with 50% of world's top semiconductor makers**
- ▶ **Licenses with four companies including recent JDA**
- ▶ **Strong team to commercialize technology**



A Better Way for Industry R&D



Industry Consortia

Little Control

Expensive &
Inefficient

Equipment OEMs

No Longer Available

Tied to
Equipment
Sales

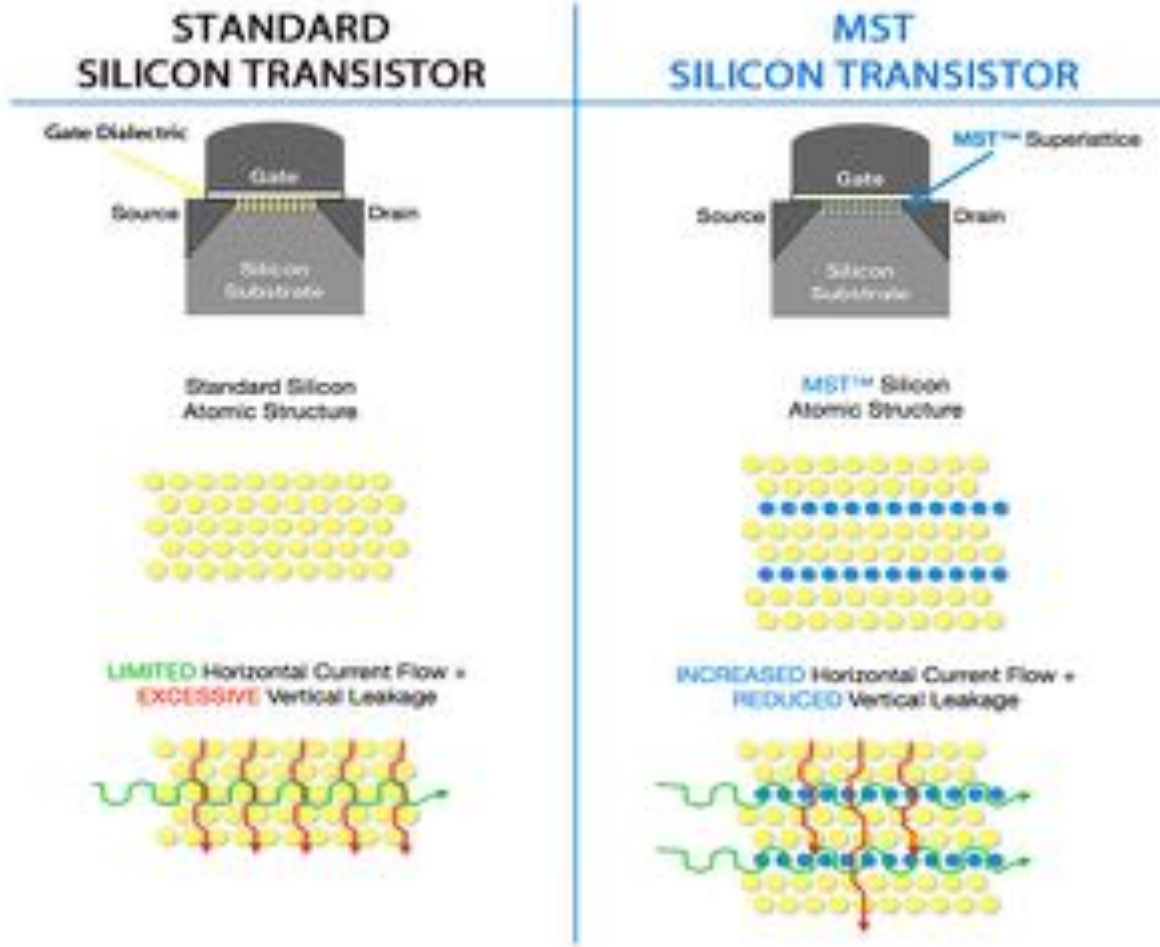
In House R&D

Large Scale,
Long Term
Investment



Targeted Innovation

**Inexpensive
& Low Risk**



Potential Benefits

► Improved Efficiency

- Higher transistor performance
- Lower power consumption
- Better reliability

► Lower cost

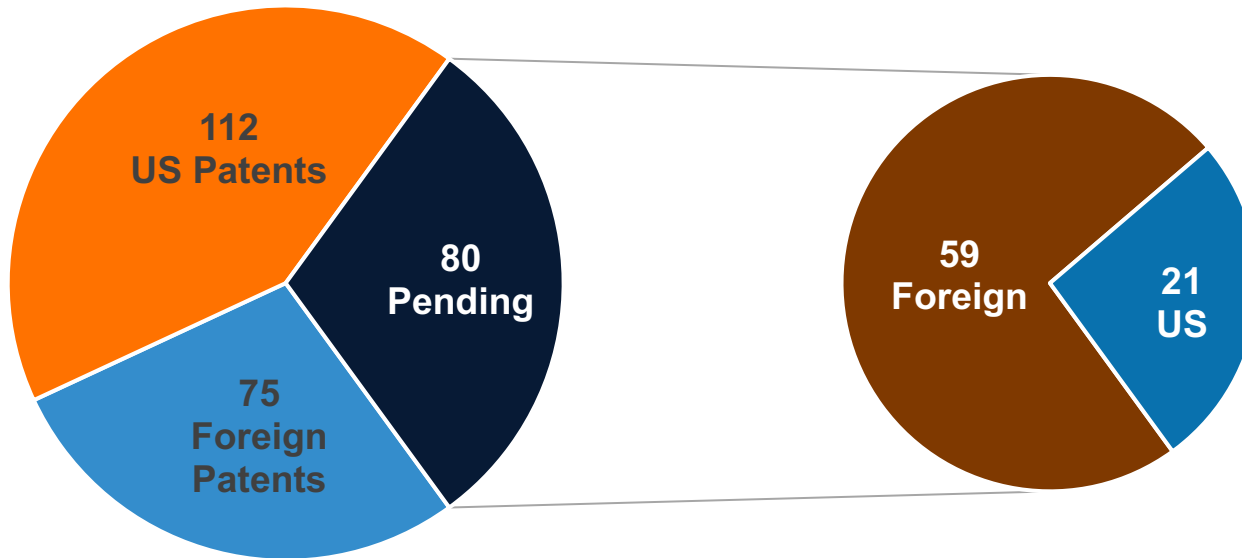
- Reduced die size
- Improved yield
- Higher throughput

► Same benefits as a node shrink

Patent Portfolio – 17% increase YoY



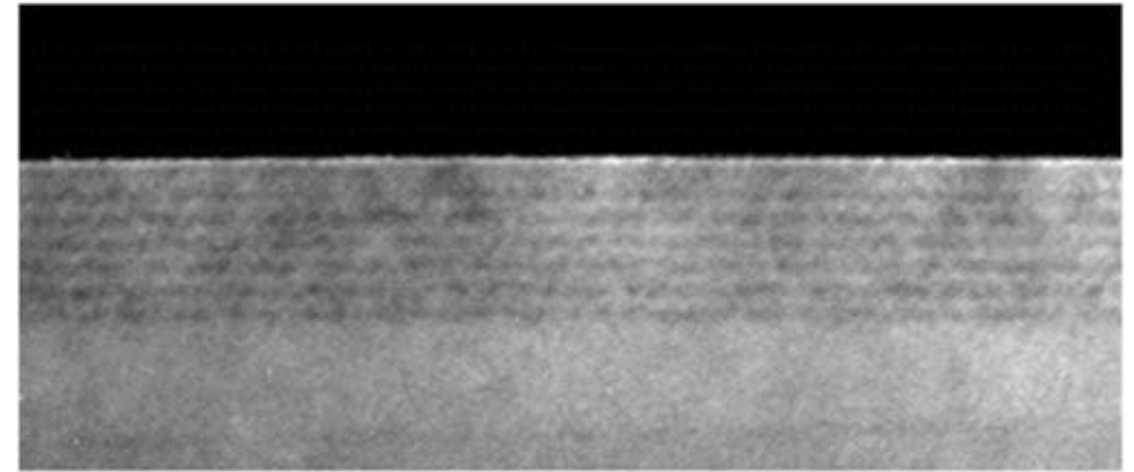
269 Patents Granted and Pending



Core MST Method and Device
MST Enabled Devices/Architecture
Next-Gen Architectures using MST

Discoverable

These distinctive layers are visible on products using MST



Extensive know-how

Extends life and value of patents

Target Customers & Partners



Integrated Device Manufacturers



Foundry



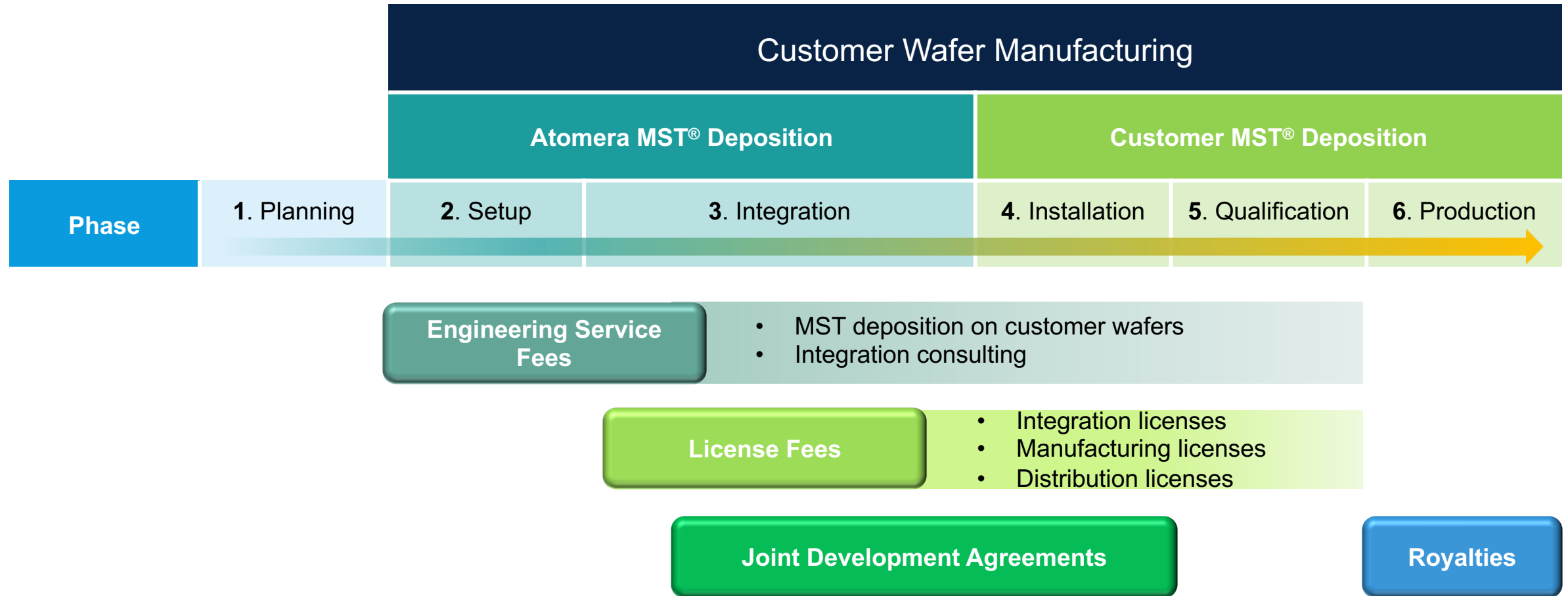
Fabless



Tool Suppliers (Partners)

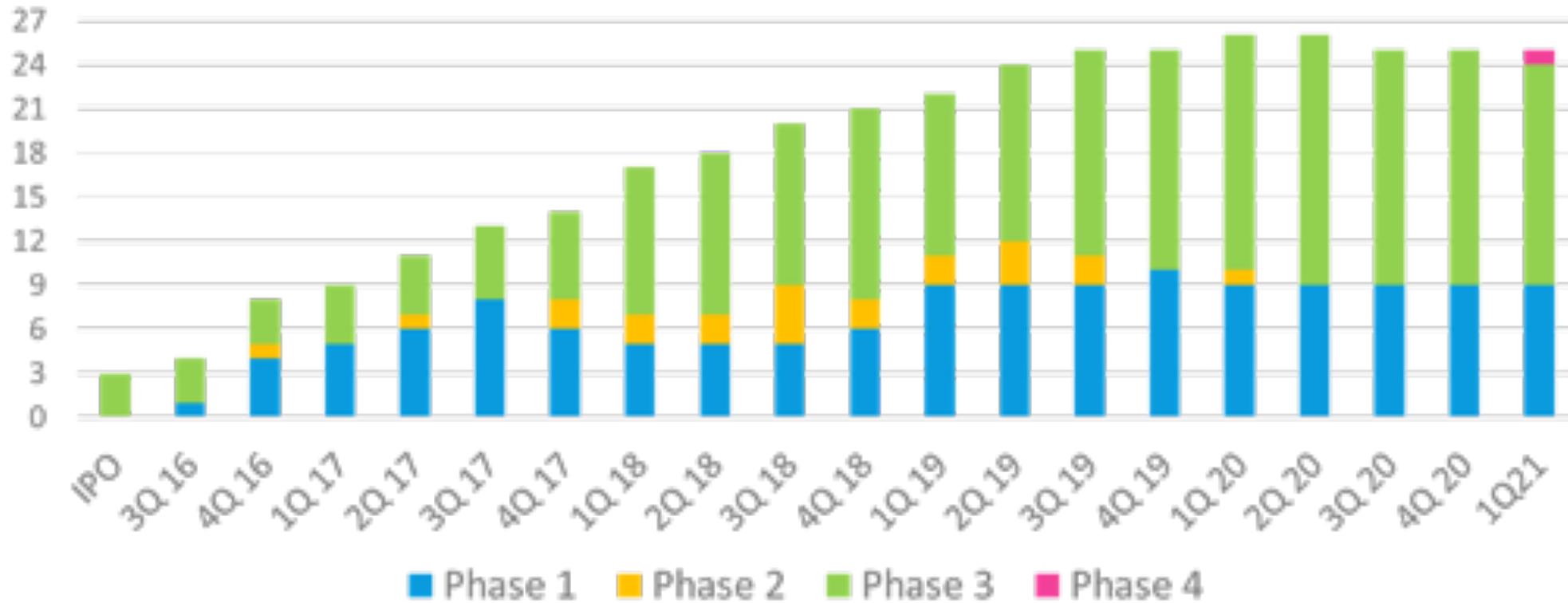


Customer Engagement & Revenue Model



Customer Pipeline

Number of Customer Engagements



- 19 customers, 25 engagements
- Working with 50% of the world's top semiconductor makers*

* At least 10 of the top 20 (IC Insights, McClean Report 2021)

Royalty Opportunity



- ▶ ~370 wafer fabs operating worldwide
- ▶ Adoption of MST in one fab can make Atomera profitable from royalties alone
 - 2021 non-GAAP OPEX guidance is \$14.00-14.5M

| Example 1 Worldwide Average Fab | |
|---|--------------|
| Monthly Fab Capacity ¹ (wafers/month) | 49,000 |
| Industry average wafer ASP - 2018 | \$1,136 |
| Annual Revenue Potential² | \$13M |
| Annual Revenue at 50% of ramp ² | \$6.7M |

| Example 2 Leading Foundry, 28nm Fab | |
|---|--------------|
| Monthly Fab Capacity (wafers/month) | 80,000 |
| Industry average 28nm wafer ASP | \$3,000 |
| Annual Revenue Potential² | \$58M |
| Annual Revenue at 50% of ramp ² | \$29M |

1. Represents wafers starts per month (200mm equiv) – 217.3M starts in 370 fabs

2. Assumes 2% royalty rate

Source: IC Insights Global Wafer Capacity 2019-2023 report, McClean Report 2019

MST Customer Business Opportunity



► Standard industry fab wafer pricing, GM, and cost

| | Price | GM% | GM\$ Increase | MST Royalty | Cost | |
|----------------|----------|-----|---------------|-------------|----------|---|
| 28nm HP wafer | \$ 3,000 | 45% | \$ - | \$ - | \$ 1,650 | |
| 28nm HP+ wafer | \$ 3,150 | | | | | \$150 price increase for +15% performance |

► Fab gets a 30% performance improvement or 25% shrink via MST

| | | | | | | |
|------------------------|----------|-------|--------|-------|----------|---|
| MST processing cost | | | | | \$ 20 | Incremental cost of depositing MST |
| 28nm HP wafer with MST | \$ 3,300 | 47.4% | \$ 214 | \$ 66 | \$ 1,736 | \$300 price increase for +30% performance |
| 28nm HP wafer with MST | \$ 3,375 | 48.5% | \$ 288 | \$ 68 | \$ 1,738 | 12.5% price increase for 25% size reduction |

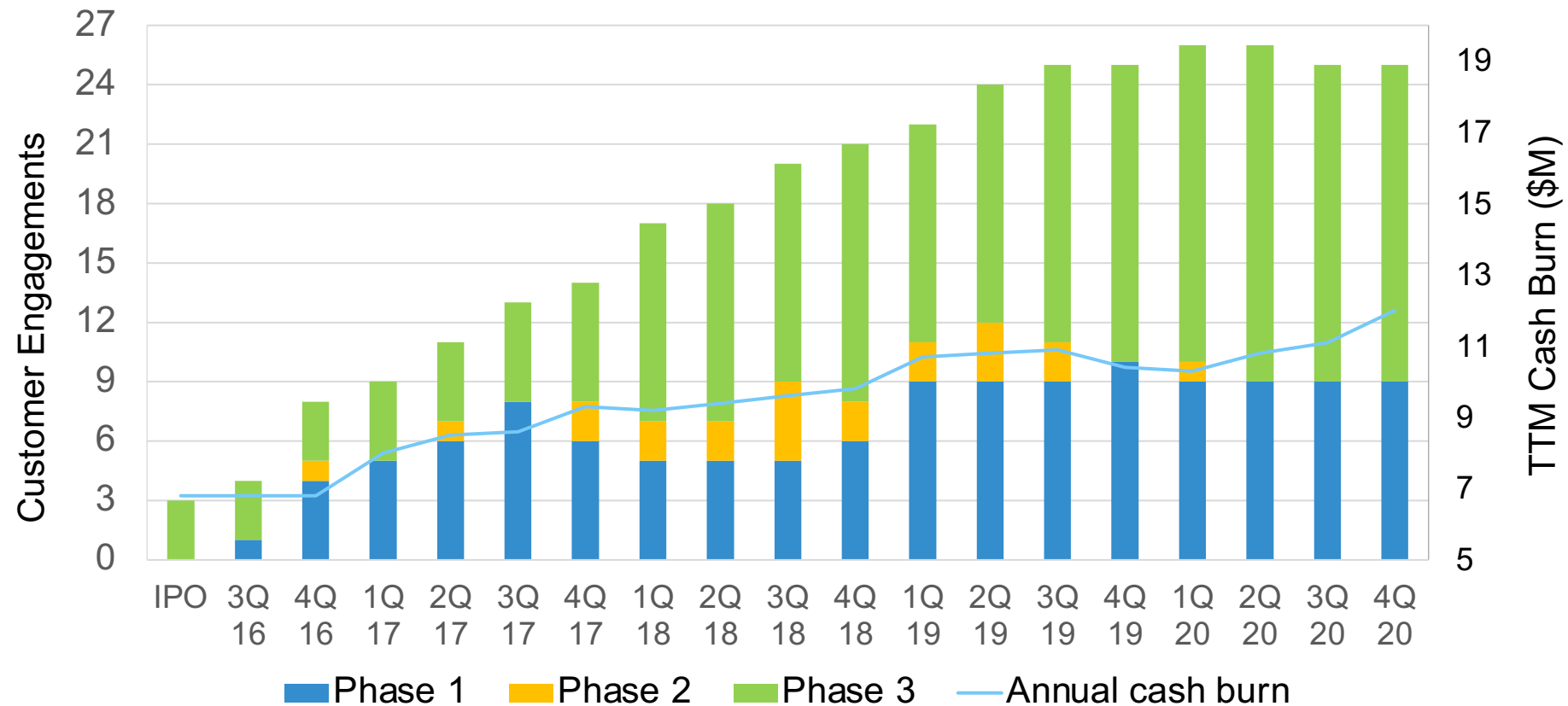
► Fabless customer benefit in die shrink case

| | Chip sales/ wafer* | GM% | GM\$ Increase | Product ASP | Die/wafer | |
|------------------------|-----------------------|-------|---------------|----------------|-----------|--|
| 28nm HP wafer | \$ 8,400 | 50.0% | \$ - | \$ 4.42 | 2,235 | Baseline business for 30mm ² chip |
| 28nm HP wafer with MST | \$ 11,279 | 62.8% | \$ 2,879 | \$ 4.42 | 3,001 | Improved financials with 25% size reduction |

► Everyone in the value chain benefits from MST technology

* Yielded

Cash Efficient Growth



Financial Review



| | Q1 '20 | Q2 '20 | Q3 '20 | Q4 '20 | FY 2020 | Q1 '21 |
|---|----------|----------|----------|----------|-----------|----------|
| GAAP Results | | | | | | |
| Revenue | \$0.06M | \$ - | \$ - | \$ - | \$0.06M | \$0.4M |
| Gross Profit | \$0.05M | \$ - | \$ - | \$ - | \$0.05M | \$0.4M |
| Operating Expense | | | | | | |
| R&D | \$2.1M | \$2.1M | \$2.0M | \$2.2M | \$8.4M | \$2.2M |
| G&A | \$1.4M | \$1.5M | \$1.3M | \$1.4M | \$5.6M | \$1.5 |
| S&M | \$0.2M | \$0.2M | \$0.2M | \$0.3M | \$0.9M | \$0.3M |
| Total Operating Expense | \$3.7M | \$3.8M | \$3.6M | \$3.9M | \$15.0M | \$4.0M |
| Net Loss | (\$3.6M) | (\$3.8M) | (\$3.6M) | (\$3.9M) | (\$14.9M) | (\$3.6M) |
| Loss Per Share | (\$0.22) | (\$0.21) | (\$0.19) | (\$0.19) | (\$0.79) | (\$0.16) |
| Reconciliation between GAAP & Non-GAAP | | | | | | |
| Net Loss (GAAP) | (\$3.6M) | (\$3.8M) | (\$3.6M) | (\$3.9M) | (\$14.9M) | (\$3.6M) |
| Stock-Based Compensation | \$0.6M | \$0.8M | \$0.8M | \$0.8M | \$3.0M | \$0.7M |
| Warrant Modification | \$0.1M | - | - | - | \$0.1M | - |
| Other income (expense) | - | - | - | - | \$0.1M | - |
| Adjusted EBITDA (Non-GAAP)* | (\$2.9M) | (\$3.0M) | (\$2.7M) | (\$3.0M) | (\$11.7M) | (\$2.9M) |

| Balance Sheet 3/31/21 | |
|-----------------------|---------|
| Cash | \$36.7M |
| Debt | - |
| Shares Outstanding | 23.1M |

*Adjusted EBITDA is a non-GAAP financial measure. A full reconciliation of GAAP and non-GAAP results is contained in our Q1 press release.

Summary



- ▶ High margin, recurring revenue financial model
- ▶ Strong technology, patent position, and balance sheet
- ▶ Traction with many top industry players and growing licensee base
- ▶ Ramping commercial license revenues



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Thank You

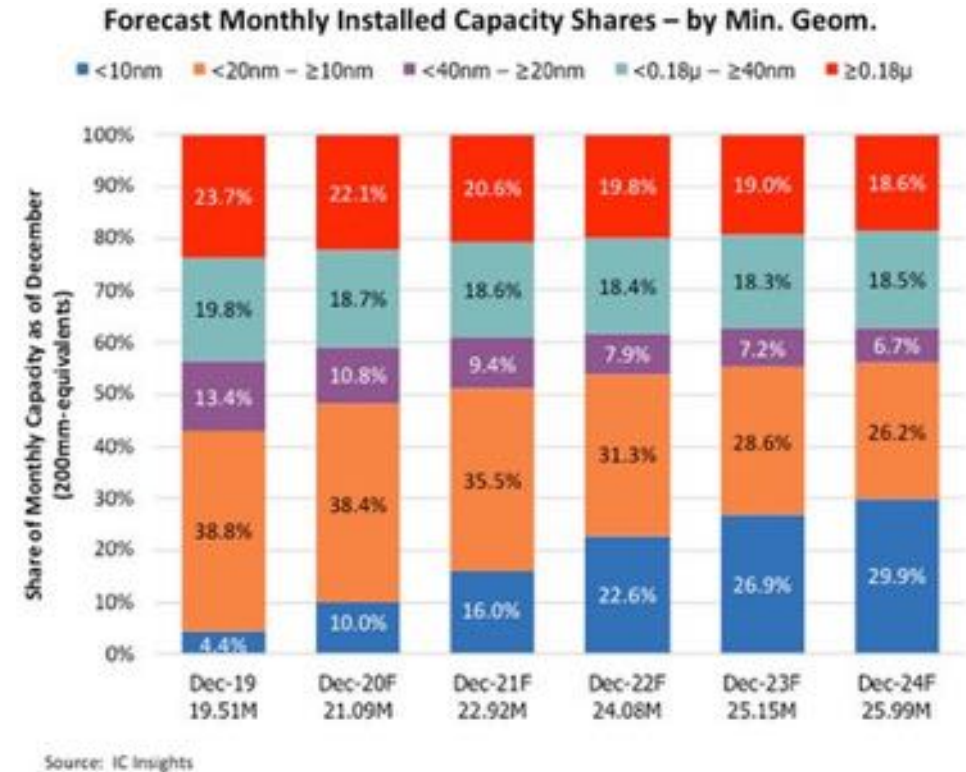


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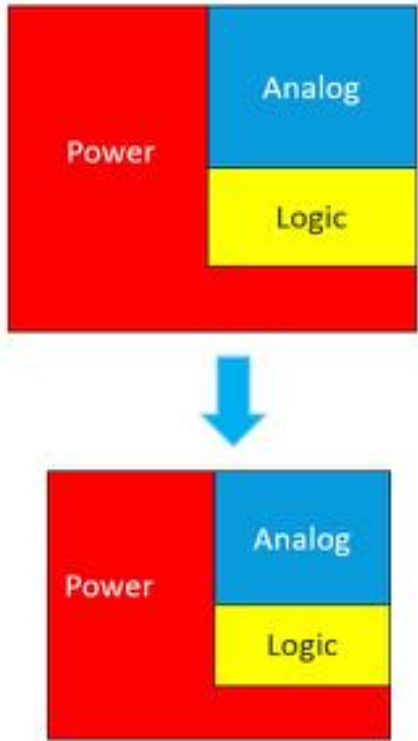
Backup Slides

Capacity challenge and opportunity

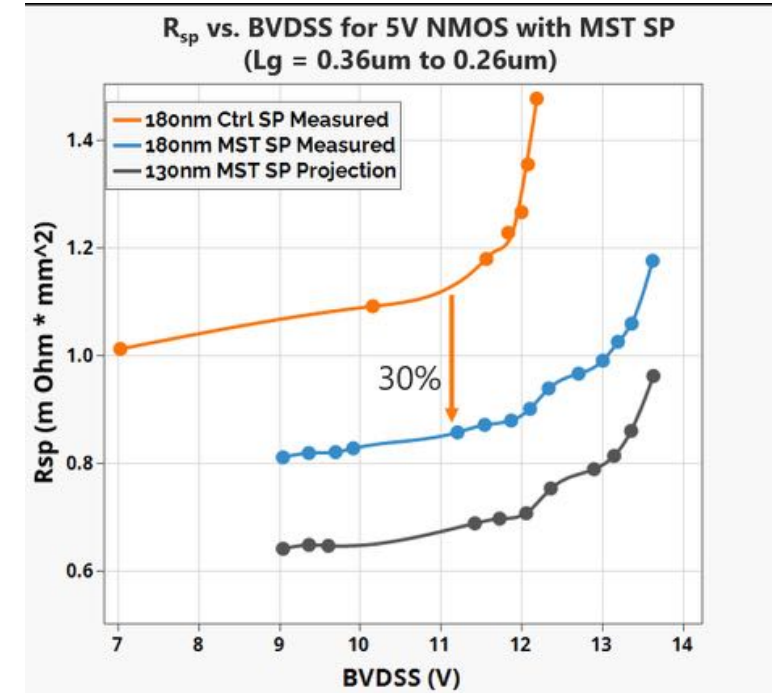
- ▶ **Chip shortages create challenge**
 - Shortages focused on legacy nodes
- ▶ **Legacy nodes made up 52% of production in 2020**
 - 41% at 40nm and below
 - 22% at 0.18u and below
- ▶ **MST provides an option to increase capacity in older production lines**



MST enables legacy capacity expansion

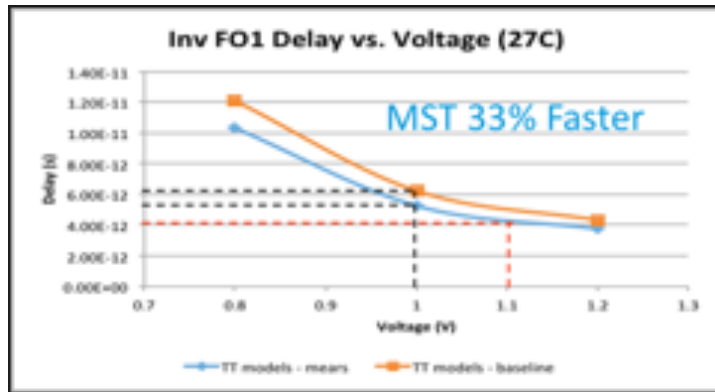


- ▶ **MST provides 30% performance advantage**
 - 0.13u analog design
 - MST vs control silicon
- ▶ **Enables a die shrink of 15-20%**
- ▶ **Smaller die means more manufacturing capacity**
 - Without the cost of building a new fab



MST 28nm benefits

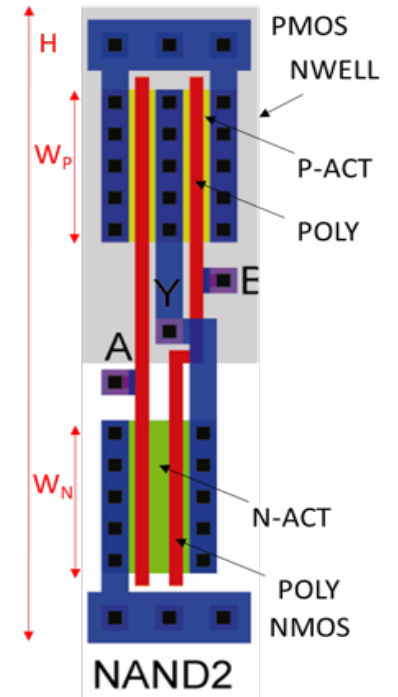
MST shows 30% higher performance



MST performance improvement due to:

- Higher electron mobility
- Improved gate oxide integrity enabling higher overdrive

- ▶ **Performance improvements due to MST can be traded for area reduction**
- ▶ **28nm PDK SPICE model used to showcase:**
 - Logic scaling with MST shows 22-25% area reduction
 - Using a NAND2 gate
 - Analog scaling with MST shows up to 21% area reduction
- ▶ **Implementation of MST on new 28nm designs can result in >20% more production capacity**
- ▶ **Allows excellent economic benefits for the whole value chain**

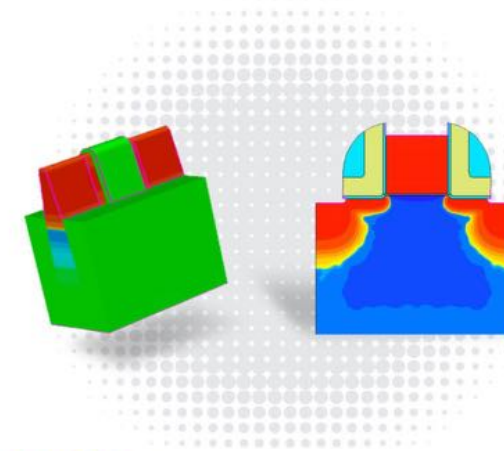


Joint Development Agreements

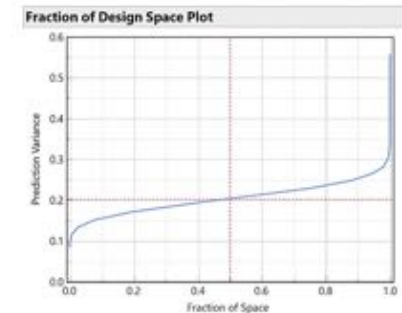
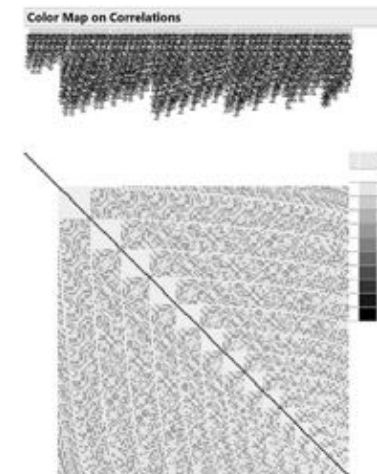


- ▶ Advantages of joint development
 - Atomera and customer engineers aligned on common goal
 - Customer “resident expert” team develops expertise on Atomera technology
 - Resident experts become natural advocates
- ▶ First JDA signed with market leading semiconductor company
 - Includes a manufacturing license, putting them in Phase 4
 - Upon completion, MST can more easily be adopted by business units
 - Each business unit is an incremental licensing opportunity

- ▶ Leading semiconductor companies use TCAD to model manufacturing processes
- ▶ MSTcad is an add-on for MST
- ▶ MSTcad can optimize complex statistical experiments to assess impact of multiple manufacturing options
- ▶ Lowers cost of MST evaluation
- ▶ Accelerates time to successful results by customers



Design Evaluation



Design Diagnostics

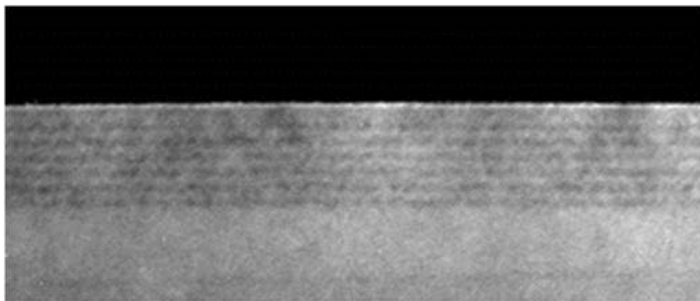
| | |
|--------------------------------|----------|
| D Efficiency | 92.30176 |
| G Efficiency | 92.28571 |
| A Efficiency | 92.28571 |
| Average Variance of Prediction | 0.203498 |
| Design Creation Time (seconds) | 0 |

MST: Mears Silicon Technology

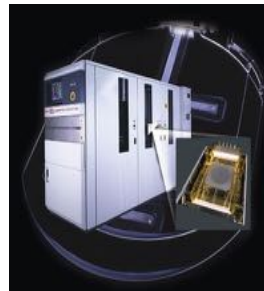


Quantum Engineered Silicon

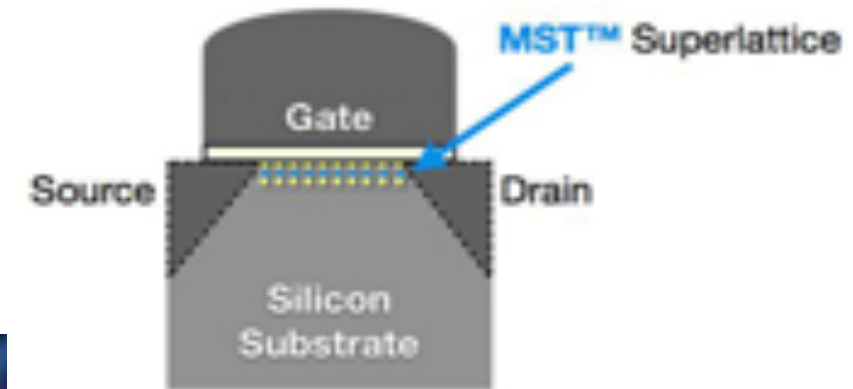
Partial Monolayers of Oxygen in Silicon



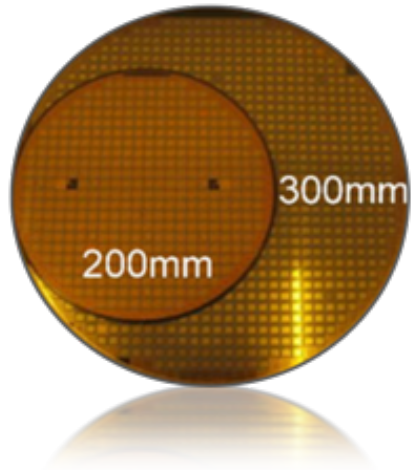
Supported by
Major Semiconductor
Tool Suppliers



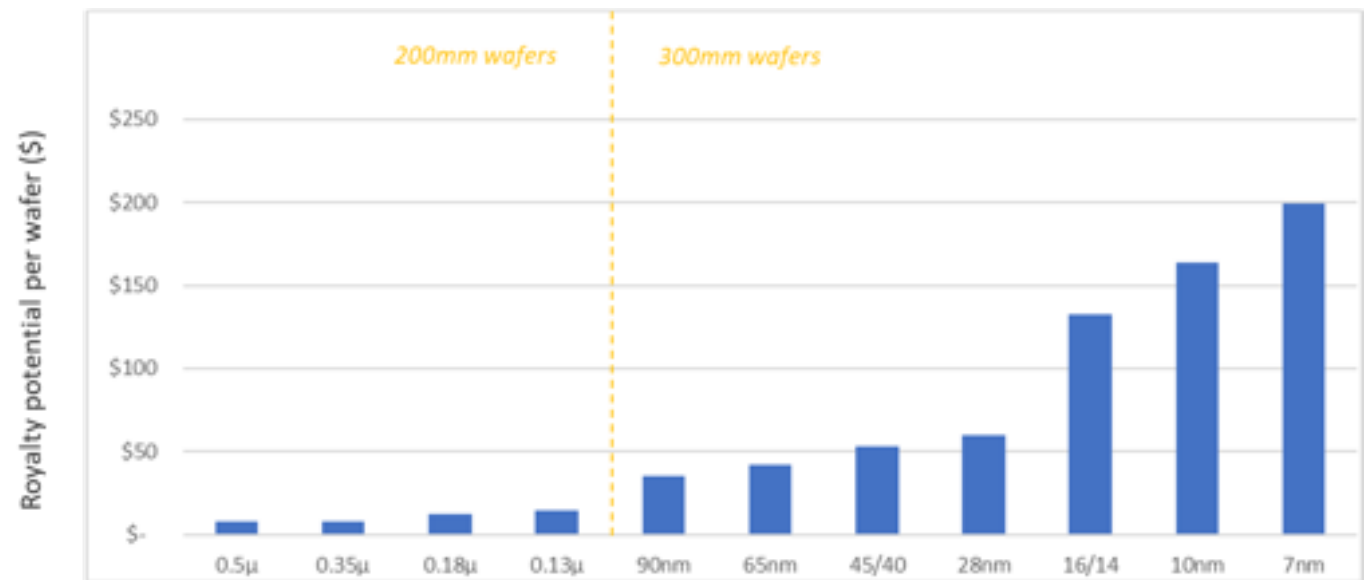
MST Enhanced Transistors



300mm Epi Tool



300mm Epi Deposition Tool

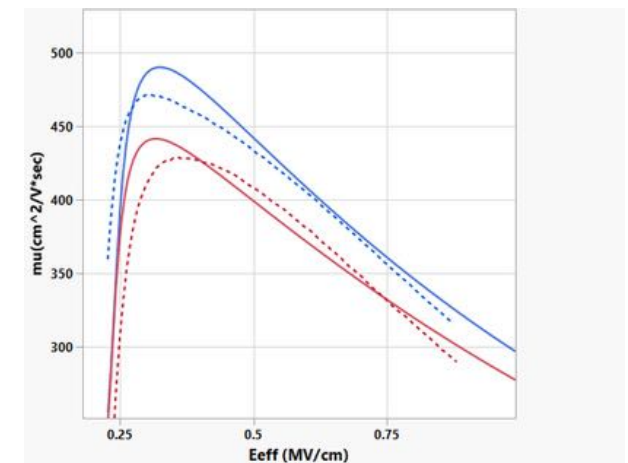
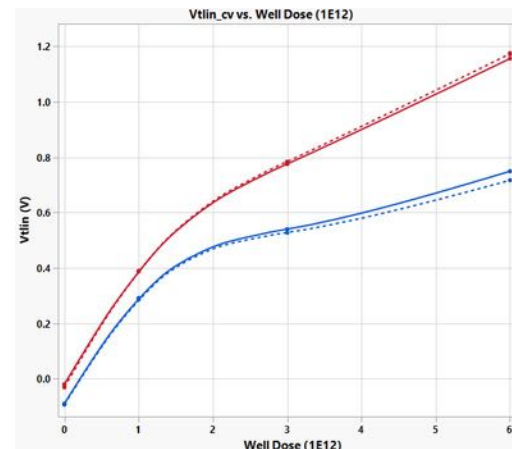
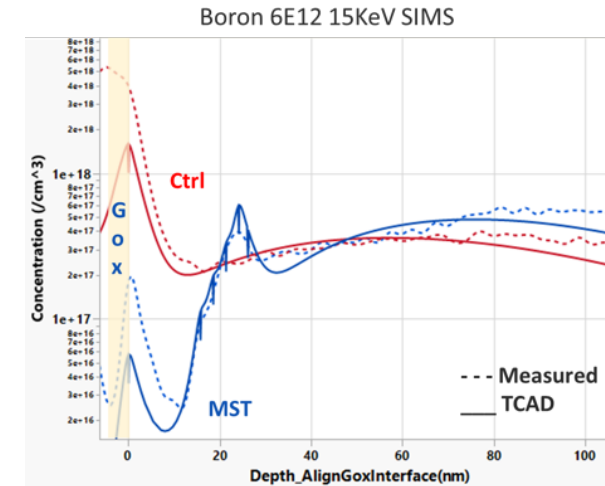


Source: The McClean Report - 2019

Atomera MSTcad™ Progress



- ▶ Leading semiconductor companies use TCAD
- ▶ MST is modelled with a TCAD add-on called MSTcad
- ▶ These plots show silicon verification of MSTcad simulations
- ▶ Enables good electrical match-up for 5V NMOS and MST SP
- ▶ Should speed time to successful results with customers



Atomera Licensees



Atomera Licenses MST Technology to Asahi Kasei Microdevices (AKM)

Highlights:

- Asahi Kasei Microdevices, a Japanese semiconductor manufacturer of high-end specialty integrated circuits (ICs) and analog products, has licensed Atomera's Mears Silicon Technology™ (MST).

Atomera Licenses MST to STMicroelectronics

Highlights:

- STMicroelectronics, a global semiconductor leader serving customers across the spectrum of electronics applications, has entered an integration license for Atomera's Mears Silicon Technology™ (MST) as a continuation of their 60GHz plan.
- The phased license agreement provides rights for STMicroelectronics to integrate Atomera MST technology in future technology.

Atomera to License MST Technology to RF Semiconductor Solution Provider for Mobile 5G Markets

The integration license agreement provides rights to develop a next-generation RF platform using MST technology.

Atomera and Market Leading Semiconductor Company Sign Joint Development Agreement for Use of MST in Future Devices

New collaboration will leverage Atomera's transistor enhancement technology to develop improvements across the manufacturer's production lines

LOS GATOS, Calif., January 5, 2021 – Atomera Incorporated (Nasdaq: ATOM), a semiconductor materials and technology licensing company, today announced it has entered into a Joint Development Agreement (JDA) with a leading semiconductor provider for integration of Atomera's Mears Silicon Technology (MST) into their silicon fabrication process. The JDA includes a manufacturing license allowing the customer to fabricate semiconductor wafers.

Asahi**KASEI**



*Large fabless
RF semiconductor
company*

*Market Leading
semiconductor
company*

MST1 vs MST2

► MST1

- Blanket technology
- Easy to integrate
- Deposited at beginning of mfg process
- Degraded by high heat in STI/Well module
- Faster time to market for low heat processes
- Used for FinFET, RFSOI, newer process nodes

► MST2

- Selective technology
 - Integrated after STI/Well so avoids highest heat
- More flexible to apply to selected areas only
- Used for 5V, Analog, older process nodes

Wafer manufacturing process

Blank Si wafer

Shallow Trench Isolation (STI) & Well module

Gate module

Source/Drain module

MST1

MST
Si

STI MST STI
Si

STI S Gate MST D STI
Si

MST2

Si

STI Si STI

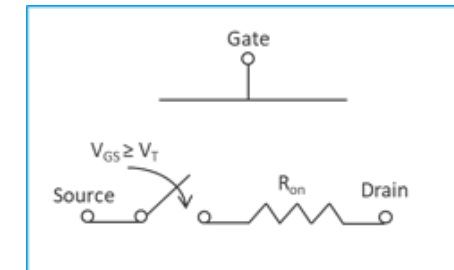
STI MST STI
Si

STI S Gate MST D STI
Si

5V Analog Breakthrough

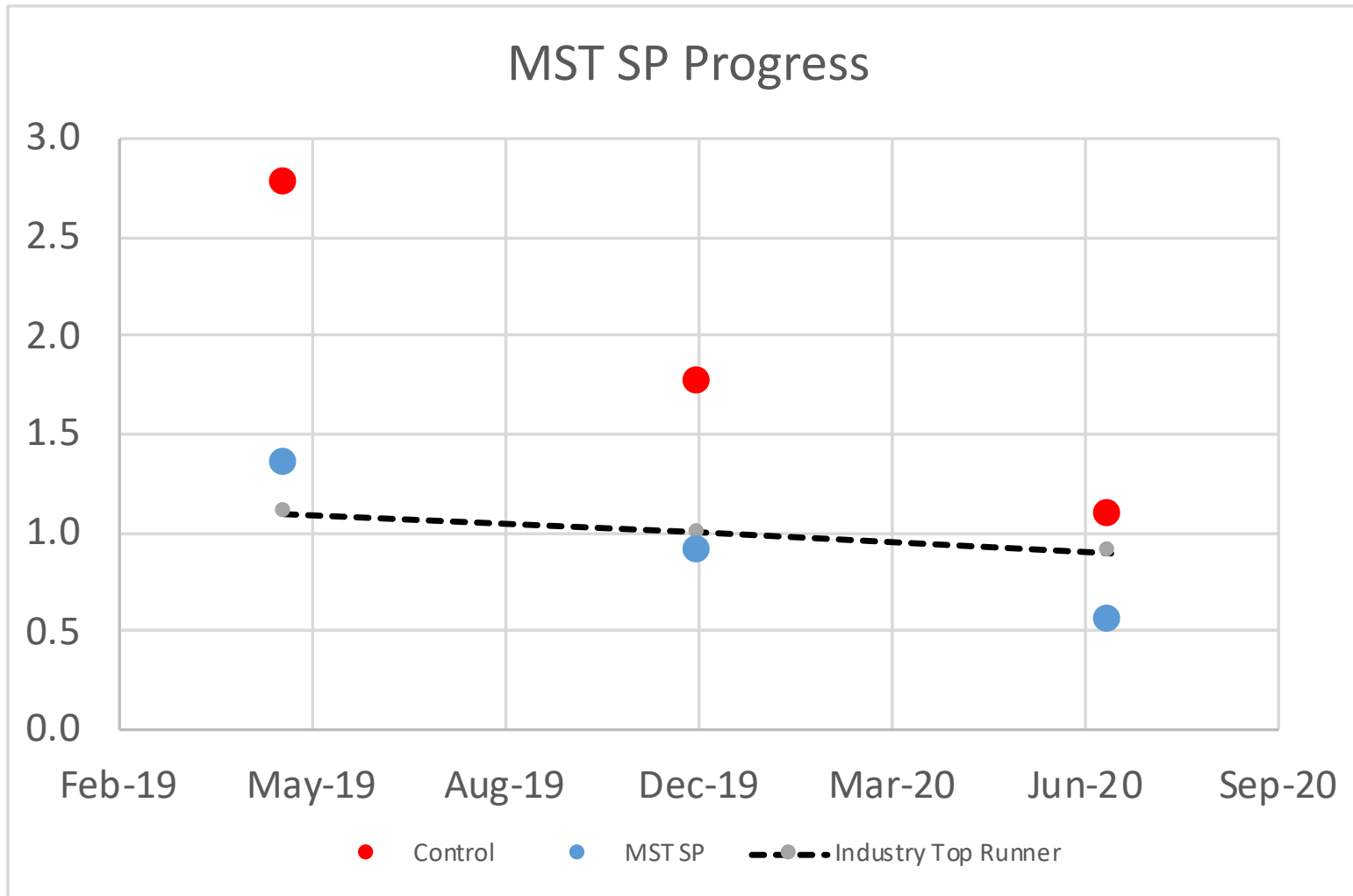


- ▶ **3. Breakthrough performance achieved on 5V analog products**
- ▶ **Large segment of the overall analog market**
- ▶ **Atomera has targeted ~20% improvement on 5V devices**
- ▶ **In April Atomera demonstrated a 50%+ improvement**
 - Using MST-SP technology
 - Relatively fast and easy to implement
- ▶ **Expected to give many business advantages**
 - Time to license, accelerated time to royalty, negotiating leverage
 - Applicable to even more markets
- ▶ **Market size: ~\$33B, or \$660M in royalties**



MST-SP Progress

R_{SP}
($m\Omega\text{-mm}^2$)



MST Matching Performance

- ▶ Transistor mismatch is an industry problem
- ▶ Certain circuit designs benefit from mismatch reduction
 - A-D convertors
 - SRAM
 - Flash
 - DRAM sense amplifiers
- ▶ MST can reduce mismatch by more than 50%
- ▶ Details available at Atomera's website
 - blog.atomera.com

